REMARKS

Initially, Applicant would like to express his appreciation to Examiner Glenn Auve for the courtesies extended to Applicant's attorney during a telephone interview on July 9, 2004. During the interview, the Examiner agreed that the Marshall reference does not teach the use of partnering signals to reset the other LIP bridge device to isolate faults as recited in Applicant's claims. Also, the Examiner agreed that the bridges in Applicant's claimed invention are peer devices to each other as distinguished from the master-slave relationship between the processors in the Marshall reference. No agreement was reached on the issue of whether there is motivation to combine the Marshall reference with other cited references for the 35 U.S.C. § 103(a) rejection.

Claims 28, 30-32, and 34-35 are pending in the application. Applicant respectfully requests additional consideration and review of the claims in view of the following remarks.

Rejections Under 35 U.S.C. § 103(a)

The Examiner has rejected claims 28, 30-32, and 34-35 under 35 U.S.C. § 103(a) as being unpatentable over Barenys et al. (U.S. 6,145,036 A) in view of various other references.

As stated in the prior amendment, an important aspect of Applicant's claimed invention is its unique means of insuring high reliability on a hierarchy of I^2C buses provided by the use of paired Layered I^2C Protocol (LIP) bridges. Partnering LIP bridges allows the host I^2C bus master to cross check data provided by the partner LIP bridge as a technique to virtually guarantee data integrity, as described on page 28, lines 5 -11 of Applicant's specification. Also, partnering allows a LIP bridge to use partnering signals to reset the other LIP bridge to isolate faults.

These aspects of the invention are set forth, for example, in claim 28, lines 15-21 which indicate that the host I^2C bus master is operable to use the recited two LIP bridges "to determine if transactions through a particular LIP bridge are corrupted ... to cross check data provided by each of said at least two LIP bridge

devices ... to use partnering signals to reset the other LIP bridge device to isolate faults."

Claims Rejected under Barenys, Khosrowpour, and Marshall

Claims 28 and 30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Barenys et al. (U.S. 6,145,036 A) in view of Khosrowpour (U.S. 6,202,115 B1), and further in view of Marshall et al. (U.S. 5,915,082 A). Applicant respectfully traverses this rejection.

There is no motivation to combine the cited references. The lack of motivation to combine these references is evidenced by the fact that there is no teaching in Barenys or Khosrowpour to suggest that there would be any improvement in Barenys' bus expansion processor system or Khosrowpour's interconnected bridge arrangement with the isolation logic as taught by Marshall. Barenys solves the problem of failures in an I^2C bus by the use of an expansion processor that performs bus isolation wherein each target device on a sub-bus can be polled to determine whether a failure exists. Khosrowpour solves the problem of failures on a bus bridge by the use of a redundant bridge arrangement that provides increased reliability and data protection, and that does not require host intervention. Marshall solves the problem of isolating failures in lockstep processor systems by the use of isolation logic that determines whether the master or slave processor has failed. Neither Barenys' expansion processor or Khosrowpour's redundant bridges are lockstep processor systems.

So why would one of ordinary skill in the art at the time the invention was made be motivated to combine Barenys and Khosrowpour with Marshall? Applicant asserts that he would not be motivated. Given that Barenys' and Khosrowpour's techniques do not suffer from the problems that Marshall addresses, the person of ordinary skill would not be led to try to improve Barenys' and Khosrowpour's techniques with Marshall's teachings. The fact that references "could" be combined is not enough. In particular, the mere fact that references can be combined or modified does not render the resulting combination obvious unless the prior art also suggests the desirability of the

combination. Applicant asserts that there is no such suggestion. Accordingly, Applicant respectfully submits that there is no motivation to combine the references and, as such, a prima facie case of obviousness has not been established.

Applicant respectfully submits that even if there were motivation to combine, which Applicant does not believe to be the case here, the proposed combination of references still falls short of teaching or even suggesting each and every limitation of Applicant's claimed invention. The Examiner proposes to combine Marshall with Barenys and Khosrowpour as the basis for rejecting Applicant's claim 28. In the Office Action, the Examiner contends that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the isolation logic, as disclosed by Marshall, in each of the at least two LIP bridges, as disclosed by Khosrowpour, as modified by Barenys, so as both of the at least two LIP bridge devices (i.e., master processor and slave processor) can analyze an error to isolate the faults (i.e., failure) and determine what corrective action is to be taken.

Briefly, Barenys discloses an I^2C bus expansion processor. The bus expansion processor is used in Barenys to isolate various buses containing expansion devices in the system and contain a bus failure to one component in the system, as disclosed by Barenys in column 1, lines 62-65.

Khosrowpour discloses two interconnected bridges that are coupled to a parent bus and to a child bus. In Khosrowpour, the first bridge performs transactions while the second bridge stores data in its cache while in a standby mode. The second bridge transmits data from its cache only when a failure occurs in the first bridge, as disclosed, for example, in column 2, lines 41 – 46 of the Khosrowpour patent.

Marshall teaches error detection, isolation, and recovery in lockstep processor systems. In Marshall, processors operate independently, but in lockstep, to process the same task with independently generated results compared in order to detect errors originating from one processor.

There are significant differences in Applicant's claimed invention and the proposed combination of Barenys, Khosrowpour and Marshall. First, as noted by the Examiner in the Office Action, Barenys does not specifically disclose two bridge devices interconnected on a parent bus as in Applicant's claim 28.

Second, neither Khosrowpour nor Barenys teach or suggest the host master is operable to "cross check data provided by each of said at least two LIP bridge devices to verify integrity of data received from said target devices" or "each of said at least two LIP bridge devices being adapted to use partnering signals to reset the other LIP bridge device to isolate faults" as recited in Applicant's claim 28.

Third, in Applicant's claimed invention, a LIP bridge operates as a slave to the host bus master on its parent bus, and a master to the target devices on its child bus. Also, the partnered LIP bridges in Applicant's claimed invention are "peer" devices to each other, meaning both LIP bridges are operable to perform the same operations in the same manner. These aspects are set forth in Applicant's claim 28, which recites "at least two LIP bridge devices being operable to transmit messages between said host bus master and said target devices" and "each of said at least two LIP bridge devices being adapted to use partnering signals to reset the other LIP bridge device to isolate faults".

Contrary to Applicant's claimed invention, the processors in Marshall are designated as either "master" processor or "slave" processor, with each "master" or "slave" having its own set of predefined operations. For example, only the master is allowed to physically send data to an I/O device, as disclosed in column 6, lines 51-55. As known by those skilled in the art, "master" devices are capable of initiating communications and exercising control functions with respect to its "slave" devices. However, Applicant believes that it is novel for a peer device to exercise such control functions over another peer device, which is not taught or suggested by Marshall.

Fourth, Applicant's claim 28 recites, "each of said at least two LIP bridge devices being adapted to use partnering signals to reset the other LIP bridge device to isolate faults". By contrast, neither Barenys, Khosrowpour, nor Marshall

teach this limitation, either when taken individually or in combination. Marshall appears to only show that the processors can disable each other as shown in Marshall's FIGs. 7-9. Marshall makes no mention of the two processors being adapted to use partnering signals to reset the other to isolate faults. As known by those skilled in the art, "reset" means to return a device to its standard or initial state, however, the device is still available for use. Disabling means that a device or features of the device are no longer available for use. Rather than resetting the processors, Marshall teaches error detection, isolation, and recovery in lockstep processor systems, wherein recovery refers to the actions that a master, slave, or the system takes to disable either processor or the lockstep feature on both processors. Therefore, the combination of Barenys, Khosrowpour and Marshall does not embody Applicant's claim 28.

With respect to claim 30, the Barenys, Khosrowpour, and Marshall combination does not teach or suggest the limitations recited in Applicant's independent claim 28 for the above-mentioned reasons. Since claim 30 depends from and therefore includes all the limitations of independent claim 28, it is therefore also believed to be allowable for the same reasons set forth above for the respective independent claim 28, as well as for other novel features.

For example, claim 30 recites, "said host bus master is operable to hold a failed interconnected LIP bridge device in a reset state in which said failed interconnected LIP bridge device is electrically removed from said child bus". The Examiner asserts that this limitation reads on Khosrowpour's teaching. Even assuming that Hub 201 in Khosrowpour is a "host master" and PCI-PCI Bridge 214 is a "LIP bridge device", the fact remains that, contrary to Applicant's claim 30, Khosrowpour does not teach holding a failed interconnected LIP bridge in a reset state in which said failed interconnected LIP bridge is electrically removed from said child bus. As known by those skilled in the art, reset means to return a device to its standard or initial state, however, the device is still available for use. Khosrowpour has no such teaching of holding a failed interconnected LIP bridge in a reset state. Also, although Khosrowpour states "even though the first bus bridge has failed or been removed", this teaching implies "physical" rather than

"electrical" removal of the failed bridge. Therefore, the combination of Barenys, Khosrowpour and Marshall does not teach or suggest all the limitations recited in claim 30.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. §103(a) rejection of claims 28 and 30.

Claims Rejected under Barenys, Khosrowpour, Marshall and Staab

Claims 31-32 and 34-35 were rejected under 35 U.S.C. §103(a) as being unpatentable over Barenys in view of Khosrowpour, and in view of Marshall et al., and further in view of Staab (U.S. 4,377,000). The Barenys, Khosrowpour, and Marshall combination does not teach or suggest the limitations recited in Applicant's independent claim 28 or intervening claim 30 for the above-mentioned reasons. Staab does not cure the deficiencies noted above for Barenys, Khosrowpour, and Marshall. Since claims 31-32 and 34-35 ultimately depend from independent claim 28, these dependent claims are therefore also believed to be allowable for the same reasons set forth above for claims 28 and 30. Therefore, the combination of Barenys with Khosrowpour, Marshall, and Staab still does not embody Applicant's claims 31-32 and 34-35.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. §103(a) rejection of claims 31-32 and 34-35.

Conclusion

In view of the remarks, Applicant submits that claims 28, 30-32 and 34-35 are in condition for allowance, and reconsideration is therefore respectfully requested. If there are any outstanding issues that the Examiner feels may be resolved by way of a telephone conference, the Examiner is invited to contact the undersigned to resolve the issues.

Respectfully submitted,
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Atts.

I hereby certify that this correspondence is being deposited in the United States Postal Service as first class mail in an envelope with sufficient postage addressed to: Mail Stop No-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on July 30, 2004.

Sharon L. Lobosco Date 7/30/04
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